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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/416,501	10/08/1999	BRIAN S. DOYLE	42390.P4514D	6248

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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/416,501	Applicant(s) Doyle
	Examiner Edgardo Ortiz	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 23, 2003* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *28-31, 33, 34, and 37* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *28-31, 33, 34, and 37* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Oct 8, 1999* is/are a) ☐ accepted or b) ☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to an appeal brief filed on May 23, 2003.

Response to Arguments

1. In view of the Appeal Brief filed on May 23, 2003, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(a) file a reply under 37 CAR 1.111 (if this Office action is non-final) or a reply under 37 CAR 1.113 (if this Office action is final); or,

(b) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CAR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CAR 1.193(b)(2).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation of a "*second single crystal substrate portion having active devices formed thereon and defining a device surface wherein the dielectric layer of the first substrate portion is bonded directly to the device surface*

of the second substrate portion", as disclosed in claim 28, must be shown or the feature(s) canceled from the claim(s). Figure 11, which shows the final structure of the claimed invention, does not show a layer (350) with active devices (352) formed thereon and defining a device surface being bonded directly to the dielectric layer of the first substrate portion (314), which is placed between layer (314) and (350).

Additionally, the limitation of a "*first device surface of the primary substrate is connected directly to the second device surface of the at least one secondary single crystal substrate such that selected ones of said active devices of said at least one secondary single crystal substrate are intercoupled via metal lines to selected ones of the first level of devices of the primary substrate*", as disclosed in claim 31, must be shown or the feature(s) canceled from the claim(s). Figure 11, which shows the final structure of the claimed invention, does not show the first device surface of the primary substrate (314) connected directly to the device surface of the at least one secondary single crystal substrate (360) such that selected ones of said active devices of said at least one secondary single crystal substrate are intercoupled via metal lines to selected ones of the first level of devices of the primary substrate.

No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 28-31, 33, 34 and 37 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant discloses on Claim 28, and its dependent claims, an apparatus including a "*a first substrate portion having a dielectric layer on a surface, a second single crystal substrate portion having active devices formed thereon and defining a device surface wherein the dielectric layer of the first substrate portion is bonded directly to the device surface of the second substrate portion*", however, the specification does not disclose nor describe a structure as claimed. Applicant also discloses on Claim 31, and its dependent claims, an apparatus including a "*first device surface of the primary substrate is connected directly to the second device surface of the at least one secondary single crystal substrate such that selected ones of said active devices of said at least one secondary single crystal substrate are intercoupled via metal lines to selected ones of the first level of devices of the primary substrate*", however, the specification does not disclose nor describe a structure as claimed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 31 and 34 are rejected under 35 U.S.C. § 102 (b) as being anticipated by Yasumoto (U.S. Patent No. 4,612,083). With regard to Claim 31, Yasumoto teaches a primary substrate (12) having a first level (14) of active devices (column 4, lines 62-64) formed thereon and defining a first device surface and at least one secondary single crystal substrate (12') having active devices formed thereon on device layer (14') and defining a second device surface, wherein the first device surface of the primary substrate is connected directly (column 7, lines 34-41 and figure 1f) to the second device surface of the at least one secondary single crystal substrate such that selected ones of said active devices of said at least one secondary single crystal substrate are intercoupled vial metal lines (20) to selected ones of the first level of devices of the primary substrate.

With regard to Claim 34, Yasumoto teaches a primary substrate (12) made of single crystal silicon (column 4, lines 64-65).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 28, 29, 33 and 37 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Sakurai (U.S. Patent No. 4,489,478) in view of Allum et.al. (U.S. Patent No. 5,622,886). With regard to Claim 28, Sakurai teaches a first substrate portion (58) having a dielectric layer (56) on a surface and a second single crystal substrate portion (44a) having active devices (53) formed thereon and defining a device surface wherein the dielectric layer of the first substrate portion is bonded directly to the device surface of the second substrate portion (see figure 7).

However, Sakurai fails to teach selected ones of active devices of the second substrate portion intercoupled via metal lines. Allum discloses a semiconductor device including a monocrystalline silicon substrate (30) having active devices (161, 163, 165, 167) formed thereon and wherein the transistors are interconnected by metal lines (see column 2, lines 39-41; column 7, lines 24-28 and figure 19). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Sakurai to include selected ones of active devices of the second substrate portion intercoupled via

metal lines, as suggested by Allum, in order to allow interconnection and integration of several transistors on a single crystal substrate.

With regard to Claim 29, Sakurai teaches a first substrate portion (58) comprising active devices (50_2) formed on the first substrate portion (see figure 7).

With regard to Claim 33, Sakurai teaches a first substrate portion (58) made of single crystal silicon (see column 6, lines 42-45).

Wih regard to Claim 37, the claim includes the limitation "*wherein the first substrate portion is formed as a film of less than an entire portion of a starting material by demarcating a film thickness through an ion implantation into the starting material and separating the first substrate portion from the starting material*", this is a product by process limitation. A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by

process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

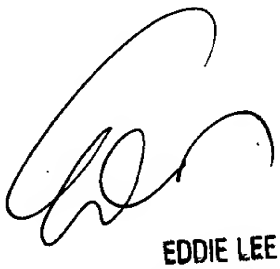
Claim 30 is rejected under 35 U.S.C. § 103 (a) as being unpatentable over Sakurai (U.S. Patent No. 4,489,478) in view of Allum et.al. (U.S. Patent No. 5,622,886) and further in view of Yasumoto (U.S. Patent No. 4,612,083). Sakurai and Allum, as stated supra, essentially disclose the claimed invention but fail to show, selected ones of the devices of the first substrate portion and selected ones of the devices of the second substrate portion are interconnected. Yasumoto discloses a semiconductor device including a first single crystal substrate (12) having a device layer (14) including active devices (column 4, lines 62-64) formed thereon and a second single crystal substrate (12') having a device layer (14') including active devices, wherein devices of the first single crystal substrate and devices of the second single crystal substrate are interconnected (column 7, lines 34-41 and figure 1f). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Sakurai and Allum to include selected ones of the devices of the first substrate portion interconnected with selected ones of the devices of the second substrate, as suggested by Yasumoto, in order to provide a three dimensional semiconductor structure on which multilayer structures are integrated within an optimal area and without sacrificing the number of semiconductor elements to be formed and interconnected.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

8/14/03



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